IN THE SPECIFICATION:

On page 2, line 13 and page 3, line 1 cancel "$V_{sat/}$" and substitute - - V_{sat} - - therefor.

On page 6, line 5 cancel "having" and insert - -has - -therefor.

On page 14, line 15 cancel "eexposing" and substitute - - exposing- - therefor.

On page 15, line 6, insert a, after "70".

On page 16, line 2, cancel "adhere is" and insert - -adheres - - therefore.

On page 18, line 10, cancel "0.05" and insert - - 0.05M - - therefor.

IN THE DRAWINGS:

Please amend FIGURE 2B in the manner set forth in the Request for Drawing Change Approval submitted concurrently herewith. Also submitted herewith is a copy of Figure 7.

IN THE CLAIMS:

Please amend the claims of the application in the following manner.

1. (Amended) A process for applying a metal [metallization interconnect structure] to a [semiconductor] microelectronic workpiece, the microelectronic workpiece including an exteriorly disposed surface having a plurality of micro-recessed structures that are defined by sidewalls, the microelectronic workpiece further including a barrier layer deposited on [a] at least a portion of the exteriorly disposed surface of the microelectronic workpiece and on at least substantial portions of the walls of the plurality of micro-recessed structures, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer [on] exterior to the barrier layer using a first deposition process, the seed layer having a thickness of less than or equal to about 500 Angstroms;

(b) enhancing the ultra-thin seed layer by depositing an additional metal using a second deposition process that is different from the first deposition process to provide an enhanced seed layer, the enhanced seed layer having a thickness at all points on sidewalls of substantially all [recessed features] micro-recessed structures distributed within the workpiece that is equal to or greater than about 10% of the nominal thickness of the enhanced seed layer [thickness] over [an] the exteriorly disposed surface of the workpiece.

In claim 9, line 1, cancel "1" and insert - - 5 - - therefor.

14. (Amended) The process of claim 4 and further comprising the step of subjecting the [semiconductor] microelectronic workpiece to a further electrochemical deposition process in an acidic electrolytic solution to complete deposition of [the] a metal to at least a thickness needed [for the formation of the interconnect structure] to substantially fill the micro-recessed structures.

15. (Amended) The process of claim 14 and further comprising the step of subjecting the [semiconductor] microelectronic workpiece to a rinsing process after electrochemical deposition in the [outline] alkaline bath and prior to the further electrochemical [copper] deposition process in an acidic electrolytic solution.

16. (Amended) In a manufacturing line including a plurality of apparatus for the manufacture of [integrated circuits] micro-sized metal structures on a microelectronic workpiece, one or more apparatus of the plurality of apparatus being used for applying metal [a copper metallization interconnect structure] to a surface of a [semiconductor] the microelectronic workpiece [used to form the integrated circuits], the one or more apparatus comprising:

means for applying a conductive ultra-thin seed layer to a surface of the [semiconductor] microelectronic workpiece using a first deposition process, the ultra-thin seed layer having a thickness of less than 500 Angstroms;

means for electrochemically enhancing the conductive ultra-thin seed layer using a second deposition process that differs from the first deposition process to [render it] thereby provide an enhanced seed layer that is suitable for subsequent electrochemical [application] deposition of the [copper interconnect metallization] metal to a predetermined thickness representing a bulk portion of the [copper interconnect] [metallization] micro-sized metal structure.

In claim 17, line for, cancel "semiconductor" and insert - -microelectronic - -therefor.

In claim 18, line 3, cancel "semiconductor" and insert - -microelectronic - -therefor.

In claim 19, line 3, cancel "semiconductor" and insert - -microelectronic - -therefor.

27. (Amended) One or more apparatus as claimed in claim 20 and further comprising means for electrochemically adding a further layer of copper over the [conductive ultra-thin] resulting enhanced seed layer by electrochemically depositing copper using an acidic copper bath.

In claim 29, line 2, cancel "semiconductor" and insert - -microelectronic - - therefor.

30. (Amended) A process for applying a [metallization interconnect] metal [structure] to a semiconductor] a surface of a microelectronic workpiece pursuant to forming one or more micro-sized metal structures thereon, the microelectronic workpiece including a barrier layer deposited on [a] at least a portion of the surface of the microelectronic workpiece [thereof], the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer, the ultra-thin metal seed layer having a thickness of less than [or equal to about] 500 Angstroms;

(b) subjecting the [semiconductor] microelectronic workpiece to an electrochemical copper deposition process in an alkaline electrolytic bath having copper ions complexed with a complexing agent such that additional copper is deposited on the ultra-thin [copper] metal seed layer to thereby [enhance the seed layer] form an enhanced seed layer that is suitable for subsequent electrochemical deposition.

43. (Amended) The process of claim 30 wherein the complexing agent is comprised of citric acid [and the citric acid in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M] .

45. (Amended) The process of claim 30 and further comprising the step of subjecting the [semiconductor] microelectronic workpiece to a further electrochemical copper deposition process in an acidic electrolytic solution to complete deposition of the copper to a thickness needed for the formation of the [copper interconnect] micro-sized metal structure.

46. (Amended) The process of claim 45 and further comprising the step of subjecting the [semiconductor] microelectronic workpiece to a rinsing process after step (b) and prior to the further electrochemical copper deposition process in [an] the acidic electrolytic solution.

Please add the following as new claims 49-69.

49. A process for applying a metal to a microelectronic workpiece pursuant to forming a micro-sized metal structure on a surface of the microelectronic workpiece, the process comprising:

(a) forming an ultra-thin metal seed layer on a surface of the workpiece using a first deposition process, the ultra-thin seed layer having a thickness of less than 500 Angstroms;

(b) enhancing the ultra-thin seed layer by depositing an additional metal layer on the ultra-thin metal seed layer using a second deposition process that differs from the first deposition process to thereby provide an enhanced seed layer that is suitable for subsequent electroplating.

50. The process of claim 49 wherein the ultra-thin metal layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.

51. The process of claim 49 wherein the ultra-thin metal seed layer of step (a) is formed in a physical vapor deposition process.

52. The process of claim 49 wherein the ultra-thin metal seed layer of step (a) is formed in a chemical vapor deposition process.

53. The process of claim 49 wherein the ultra-thin seed layer is enhanced in step (b) by electrochemically depositing the additional metal layer.

54. The process of claim 52 wherein the microelectronic workpiece comprises a barrier layer on which the ultra-thin seed layer is formed and wherein the additional metal layer is electrolytically deposited using an alkaline electrolytic plating solution that includes a complexing agent.

55. The process of claim 53 and further comprising the step of electrolytically depositing a metal layer on the surface of the enhanced seed layer in an acidic electrolytic plating solution.

56. The process of claim 54 and further comprising the step of rinsing the microelectronic workpiece after electrolytically enhancing the ultra-thin seed layer in the alkaline electrolytic plating solution and prior to subjecting the microelectronic workpiece to the acidic electrolytic plating solution.

57. The process of claim 50 wherein the ultra-thin metal seed layer of step (a) is formed in a physical vapor deposition process.

58. The process of claim 50 wherein the ultra-thin metal seed layer of step (a) is formed in a chemical vapor deposition process.

59. The process of claim 50 wherein the ultra-thin seed layer is enhanced in step (b) by electrochemically depositing the additional metal layer.

60. The process of claim 59 wherein the microelectronic workpiece comprises a barrier layer on which the ultra-thin seed layer is formed and wherein the additional metal layer is electrolytically deposited using an alkaline electrolytic plating solution that includes a complexing agent.

61. The process of claim 60 and further comprising the step of electrolytically depositing a metal layer on the surface of the enhanced seed layer in an acidic electrolytic plating solution.

62. The process of claim 61 and further comprising the step of rinsing the microelectronic workpiece after electrolytically enhancing the ultra-thin seed layer in the alkaline electrolytic plating solution and prior to subjecting the microelectronic workpiece to the acidic electrolytic plating solution.

63. In a manufacturing line including a plurality of apparatus for the manufacture of microelectronic circuits or components, one or more apparatus of the plurality of apparatus being used for applying interconnect metallization in a damascene process to a surface of a microelectronic workpiece used to form the microelectronic circuits or components, the one or more apparatus comprising:

means for applying an ultra-thin metal seed layer to a surface of the semiconductor workpiece using a physical vapor deposition process, the ultra-thin metal seed layer having a thickness less than 500 Angstroms;

means for electrochemically enhancing the conductive ultra-thin seed layer to render it suitable for subsequent electrochemical application of a metal to a predetermined thickness representing a bulk portion of the interconnect metallization.

64. A process for applying a metal to a microelectronic workpiece, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer using a first deposition process, the first deposition process physically anchoring the ultra-thin metal seed layer to an underlying layer, the ultra-thin metal seed layer having a thickness that is less than 500 Angstroms;

(b) enhancing the ultra-thin seed layer by electrochemically depositing an additional metal on the ultra-thin seed layer using a second deposition process that is different from the first deposition process to form an enhanced seed layer;

(c) electrolytically depositing a metal on the enhanced seed layer under conditions in which the deposition rate of the electrolytic deposition process is greater than the deposition rate of the process used in enhancing the ultra-thin seed layer.

65. A process for filling a micro-recessed structure disposed in a surface of a microelectronic workpiece with a metal, the microelectronic workpiece including a barrier layer deposited on at least a portion of the upper surface thereof and on surfaces of the plurality of micro-recessed structures, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer using a physical vapor deposition process, the ultra-thin metal seed layer having a thickness that is less than or equal to about 500 Angstroms;

(b) enhancing the ultra-thin seed layer by electrolytically depositing additional metal on the ultra-thin metal seed layer using an alkaline electroplating solution to thereby form an enhanced seed layer.

66. The process of claim 65 and further comprising the step of substantially filling the micro-recessed structures with a metal in an electrolytic deposition process using an acidic electroplating solution.

67. A process for applying a metal to a microelectronic workpiece, the microelectronic workpiece including a surface in which are disposed a plurality of micro-recessed structures, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the surface of the microelectronic workpiece, including the walls of the plurality of micro-recessed structures, the ultra-thin metal seed layer being formed using a first deposition process and having a thickness of less than or equal to about 500 Angstroms;

(b) enhancing the ultra-thin seed layer by depositing an additional metal using a second deposition process that is different from the first deposition process to provide an enhanced seed layer.

68. A process for applying a metal to a microelectronic workpiece, the microelectronic workpiece including an exteriorly disposed surface having a plurality of micro-recessed structures that are defined by sidewalls, the microelectronic workpiece further including a barrier layer deposited on at least a portion of the exteriorly disposed surface of the microelectronic workpiece and on at least substantial portions of the walls of the plurality of micro-recessed structures, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer exterior to the barrier layer using a first deposition process;

(b) enhancing the ultra-thin seed layer by depositing an additional metal using a second deposition process that is different from the first deposition process to provide an enhanced seed layer, the additional metal being formed from a metal comprising the same metal used to form the ultra-thin seed layer, the enhanced seed layer having a thickness at all points on sidewalls of substantially all micro-recessed structures distributed within the workpiece that is equal to or greater than about 10% of the nominal thickness of the enhanced seed layer over the exteriorly disposed surface of the workpiece; and

(c) electroplating a metal onto the enhanced seed layer so as to fill the micro-recessed structures.

69. A process for applying a metal to a microelectronic workpiece, the microelectronic workpiece including a surface in which are disposed a plurality of micro-recessed structures, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the surface of the microelectronic workpiece, including the walls of the plurality of micro-recessed structures, the ultra-thin metal seed layer being formed using a first deposition process;

(b) enhancing the ultra-thin seed layer by depositing an additional metal using a second deposition process that is different from the first deposition process to provide an enhanced seed layer, the additional metal being formed from a metal comprising the same metal used to form the ultra-thin seed layer; and

(c) electroplating a metal onto the enhanced seed layer so as to fill the micro-recessed structures.